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# MULTI-TAP, DIGITAL-PULSE-DRIVEN MIXER

This application claims the priority under 35 U.S.C. 119(e)(1) of copending U.S. provisional application number 60/195,926 filed on April 10, 2000.

## FIELD OF THE INVENTION

The invention relates generally to frequency channel communications and, more particularly, to mixers for downconverting the frequency of a received communication signal.

## BACKGROUND OF THE INVENTION

Among conventional RF-to-IF (radio frequency-to-intermediate frequency) mixers, zero-IF implementations have the inherent problem of LO (local oscillator) leakage through the mixer to the RF input, which then gets downconverted inside the mixer. One solution currently in discussion to solve this problem is to use a sub-harmonic pumped mixer for the down conversion. Such a mixer either requires very high LO drive currents or suffers from undesirably high noise figures. The sub-harmonic

pumped mixer also generates the needed RF frequency internally, so there is still a LO leakage problem with this architecture. For low IF implementations, the realization of 90 degree phase splitters is one of the biggest challenges.

It is therefore desirable to provide a mixer that avoids the aforementioned disadvantages of conventional approaches.

The present invention provides a multi-tap, digital-pulse-driven mixer which advantageously avoids LO leakage by shifting the LO frequency out of the receive frequency band, and which advantageously realizes low noise figures by the use of digital pulses as mixer drive signals.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIGURE 1 diagrammatically illustrates an exemplary mixer embodiment according to the invention.

FIGURE 2 diagrammatically illustrates exemplary embodiments of the switches and anti-aliasing filters of FIGURE 1.

FIGURE 3 graphically illustrates an exemplary timing relationship between the RF signal of FIGURE 1 and the sampling pulse signal of FIGURE 1.

FIGURE 4 diagrammatically illustrates an exemplary embodiment of the delay element section of FIGURE 1.

FIGURE 5 graphically illustrates examples of various signals from FIGURE 4, their mutual timing relationships, and their respective timing relationships relative to the RF signal of FIGURE 1.

FIGURE 6 illustrates in tabular format exemplary operations of the router of FIGURE 1.

FIGURE 7 illustrates exemplary operations which can be performed by the embodiments of FIGURES 1-6.

FIGURE 8 illustrates exemplary operations which can be performed by the embodiments of FIGURES 1-6.

FIGURES 9 and 10 graphically illustrate exemplary signals of FIGURE 1.

**DETAILED DESCRIPTION**

If a mixer, such as an RF-to-IF mixer, is driven using a digital pulse with rise and fall times that are small compared to the pulse width, the needed voltage swing can be reduced. For a resistive mixer, which is equivalent to a sampling switch, the needed voltage swing above $V_{th}$ is determined by the $g_m$ saturation at low $V_{ds}$, because the maximum signal swing at that point in, for example a wireless system, is limited to 50 mV. Therefore 150 to 200 mV will be sufficient. The voltage swing needed below $V_{th}$ is determined by the off current needed and will be around 300 - 400 mV. Therefore a total voltage swing of 500 - 600 mV will be sufficient. This voltage swing can be realized, for example, by local power regulation of the driving inverter. When comparing that situation to, for example, an analog mixer drive circuit with a sinusoidal drive waveform and wherein the needed overdrive voltage is small, one can obtain an equivalent analog voltage amplitude by calculating waveforms with equal voltage derivatives at zero crossing points:

Equation 1

$$dV_{ana}/dt = dV_{dig}/dt$$

Equation 2

$$d(V_{pp}/2*\sin(\omega t)) = V_S/t_{tr}$$

Equation 3

$$V_{pp} = V_S*1/\pi*(T_{RF}/t_{tr})$$

where $V_S$ is the digital voltage swing and $t_{tr}$ is the digital transition (rise/fall) time.

Equation 3 shows that a factor of $1/\pi*(T_{RF}/t_{tr})$ is gained with respect to voltage swing. For typical inverter delays of 20 psec for a conventional Texas Instruments deep-submicron CMOS process with $L_g$= 0.13 micrometers, the gain with a digital-pulse-driven mixer can be around a factor of 10 compared to an analog implementation.

The current consumption needed by a digital drive circuit can also be calculated. The mean current consumption for one digital pulse with a repetition rate $T_{rep}$, is given by:

Equation 4

$$I_{mean} = 2*V_S*(C_{load} + C_{par} + C_{inv})/T_{rep}$$

where $C_{load}$ is the capacitance of the sampling switch, $C_{par}$ is the parasitic capacitance of the wiring and $C_{inv}$ is the output capacitance of, for example, a driving inverter. It is important to notice that the current consumption is independent of $t_{tr}$, while the noise figure of the circuit goes down with $t_{tr}$. The size of $C_{load}$ is determined by the needed on resistance $R_{on}$ of the sampling switch, which should be a factor of 10 lower than the input

impedance of the first IF amplifier. To meet typical noise floor requirements with an exemplary LNA gain of 20 dB, an input impedance around 500 Ohm or a sample switch $g_m$ of around 50 Ohm is required. With a typical $g_m$ of 3mS/um, a 50 um wide transistor is needed, which has an input capacitance of 40 fF. The typical output capacitance of an inverter is very similar, and the interconnection parasitic can be kept below 5 fF with suitable attention to the layout. This gives total current consumption of 0.25mA.

FIGURE 1 diagrammatically illustrates an exemplary embodiment of a mixer according to the present invention for downconverting a communication signal from RF (radio frequency) to IF (intermediate frequency). The exemplary embodiment of FIGURE 1 is a digital-pulse-driven mixer which can, accordingly, realize one or more of the aforementioned advantageous characteristics associated with a digital-pulse-driven design. In FIGURE 1, an RF communication signal input 22 is applied to a low noise amplifier (LNA) 18 whose output 23 is in turn applied to a plurality of sampling switches 19. In response to a plurality of digital control signals 16, the sampling switches at 19 sample the amplified RF signal 23. The switches 19 output the sampled RF signal at 20 to anti-aliasing filters 21, which produce the IF signal.

A local oscillator 11 produces a synthesized frequency signal 12 having a frequency $F_{LO}$. This local oscillator signal 12 is input to a digital pulse generator 13

which produces in response thereto a sampling pulse signal SPS which is in turn input to a section of delay elements 15. A router 17 is coupled to receive signals 14 from the outputs of the respective delay elements at 15, and the router 17 also receives the sampling pulse signal SPS. The router 17 suitably routes the signals 14 and the sampling pulse signal SPS to drive the various digital control signals 16 and thereby control the sampling switches 19 as desired. The router 17 and switches 19 thus provide a sampler for sampling the RF signal 23.

FIGURE 2 diagrammatically illustrates exemplary embodiments of selected portions of the mixer of FIGURE 1. In the example of FIGURE 2, the switches 19 are provided as CMOS pass gates controlled by the digital signals 16 produced by the router 17. The exemplary embodiment of FIGURE 2 includes n switches S1 - Sn, where n = M x 4 and M is an integer. The switches 19 are partitioned into M groups of 4 switches, the switches S1 - S4 being exemplary of one such group. As shown in FIGURE 2, switch S1 samples the RF input signal 23 at a phase of 0°, switch S2 samples at a phase of 90°, switch S3 samples at 180°, and switch S4 samples at 270°. Similarly, switches S5, S9 ... Sn–3 sample at 0°, switches S6, S10, ... Sn–2 sample at 90°, switches S7, S11, ... Sn-1 sample at 180°, and switches S8, S12, ... Sn sample at 270°. The sampled phases are input to appropriate anti-aliasing filters 21 which recombine the sampled phases. In the

example of FIGURE 2, the anti-aliasing filters 21 are conventional third-order low-pass filters, one of which includes an in-phase IF amplifier I that receives phases 0° and 180°, and the other of which includes a quadrature IF amplifier Q that receives phases 90° and 270°. The outputs of the filters 21 can be applied to, for example, a conventional ΣΔ multi-bit A/D converter (not shown).

Referring also to FIGURE 1, n–1 of the n digital control signals 16 are provided as delayed versions of a pulse (or pulses) of the sampling pulse signal SPS, and one of the control signals 16 is the pulse (or one of the pulses) from which the delayed versions are produced. For example, if switch S1 is controlled by a given SPS pulse, then switches S2 - Sn can be driven by respective delayed versions of that SPS pulse. If each of the four phases is sampled during each cycle of the RF input signal 23, then a new SPS pulse will be needed approximately every M ( = n/4) cycles of the signal 23.

Advantageously according to the invention, the SPS pulses have a pulse width which is approximately equal to but slightly larger than the half period of the RF input signal, as illustrated generally in FIGURE 3. The FIGURE 3 relationship between the SPS pulse width and the half period of the RF input signal can advantageously reduce the noise figure of the mixer, because the switching point of at least some of the pulses which control the sampling operations of switches S1 - Sn (see also FIGURE 2) can be made

exactly aligned with the zero crossings of the RF signal 23, which allows implementation of coherent detection. As one example, the SPS pulse width can be [(n+1)/n] x (half period of RF input signal). In this example, the relationship of the frequency $F_{LO}$ of the local oscillator output 12 (see also FIGURE 1) to the frequency $F_{RF}$ of the RF input signal should be: $F_{LO}=F_{RF}$ x [n/(n+1)]. The digital pulse generator 13 of FIGURE 1 can then utilize well-known conventional techniques to produce the sampling pulse signal SPS having a pulse duration of [(n+1)/n] x (half period of RF input signal) and such that the SPS pulse is repeated every M cycles of the local oscillator output 12.

Due to the above-described exemplary relationship between $F_{LO}$ and $F_{RF}$, the length of each cycle of the local oscillator output 12 will be [1 + (1/n)] x (period of the RF input signal). Recalling that the spacing between SPS pulses is M cycles of the local oscillator output 12, and recalling that M = n/4, the timing relationship of the (j+1)th SPS pulse with respect to the RF input signal will be delayed by ¼ of a cycle of the RF input signal when compared to the timing relationship of the immediately preceding (jth) SPS pulse with respect to the RF input signal. This ¼ of a cycle delay is due to the fact that the local oscillator signal 12 "loses" (1/n)th of a cycle (relative to the RF signal 23) during each of the M = n/4 cycles between SPS pulses, and $\frac{1}{n} x \frac{n}{4} = \frac{1}{4}$. This delay

between adjacent SPS pulses can be compensated for in the design of the delay elements 15 and the router 17 of FIGURE 1, as described in detail below.

FIGURE 4 diagrammatically illustrates an exemplary embodiment of the delay element section 15 of FIGURE 1. The embodiment of FIGURE 4 includes a plurality of delay elements DE1 - DEn–1 and DEC connected in series to form a delay chain. In some embodiments, each of the illustrated delay elements provides a delay of ¼ cycle of the RF input signal 23. Referring also to FIGURES 1 and 2, the router 17 can route SPS to control switch S1, and can also route the outputs of delay elements DE1 - DEn–1 to respectively control switches S2 - Sn. Because each of the delay elements delays the input SPS pulse by ¼ of a cycle of the RF input signal, the SPS pulse and the respective ¼ cycle delayed versions thereof can control switches S1 - Sn to sample at the appropriate phases of the RF input signal.

For example, the SPS pulse can be used to control switch S1 to sample at 0°, the output of delay element DE1 can be used to control switch S2 to sample at 90°, the output of delay element DE2 can be used to control switch S3 to sample at 180°, and the output of delay element DE3 can be used to control switch S4 to sample at 270°. The delay element DE4 can be used to control the next switch S5 (not illustrated in FIGURE 2) to sample at 0° of the next cycle of the RF input signal 23, and so on until delay

element DEn–1 controls switch Sn to sample at 270° of the Mth cycle of signal 23. This exemplary operation is illustrated generally in FIGURE 5.

As shown in FIGURE 5, the SPS pulse 51 provides for sampling at 0° of cycle 1 of the RF signal 23 and the sampling continues at 90° phase increments through the sampling at 270° of cycle M by delay element DEn – 1. As mentioned above, however, after M cycles of the local oscillator output 12, the timing relationship of the next SPS pulse 52 with respect to the RF input signal 23 will be delayed by ¼ cycle (90° phase) as compared to the timing relationship of the SPS pulse 51 with respect to the RF input signal 23. Thus, as illustrated in FIGURE 5, the SPS pulse 52 will not be available to sample at 0° of cycle M+1 of the RF input signal, but rather will be available ¼ of a cycle later to sample at 90° of cycle M+1. Accordingly, the router 17 of FIGURE 1 can route the SPS pulse 52 to switch S2 of FIGURE 2 for sampling at 90° of cycle M+1. The sampling at 0° of cycle M+1 is controlled by the pulse output from the compensating delay element DEC, which the router 17 routes to control the switch S1 of FIGURE 2. The output of DE1 is routed to switch S3 to sample at 180° of cycle M+1, the output of DE2 is routed to switch S4 to sample at 270° of cycle M+1, and so on as illustrated in FIGURE 5.

FIGURE 6 illustrates in tabular format exemplary operations which can be performed by the router 17 of FIGURE 1 to control the sampling switches at 19 in FIGURE 2. The example of FIGURE 6 is for n=16 switches partitioned into M = 4 groups of 4 switches each, each group of 4 switches operable for sampling the desired 4 phases of an associated cycle of the RF input signal. Also in the FIGURE 6 example, $F_{LO} = F_{RF} \times [n/(n+1)] = F_{RF} \times (16/17)$. As shown in FIGURE 6, for a given cycle K of the RF input signal, the SPS pulse (e.g., 51 in FIGURE 5) is used to control switch S1 to sample at 0°, and the respective delay elements DE1 - DE15 are used to control the respective switches S2 - S16 to sample as shown in cycles K through K+3. In cycle K+4, the output of DEC is used to control switch S1 to sample at 0°, the SPS pulse (e.g., 52 in FIGURE 5) is used to control switch S2 to sample at 90°, and the respective outputs of DE1 - DE14 are used to control the respective sampling operations of the switches S3 - S16 in the remainder of cycle K+4 and in cycles K+5 through K+7.

In cycle K+8, the output of DE15 is used to control switch S1 to sample at 0°, the output of DEC is used to control switch S2 for sampling at 90°, and the SPS pulse is used to control switch S3 for sampling at 180°. The output of DE1 is used to control S4 for sampling at 270° during cycle K+8, and the respective outputs of DE2 - DE13 are used to

control the sampling operations of the respective switches S5 - S16 in cycles K+9 through K+11. In cycle K+12, the output of DE14 drives switch S1 to sample at 0°, the output of DE15 drives switch S2 to sample at 90°, the output of DEC drives switch S3 to sample at 180°, and the SPS pulse drives S4 to sample at 270°. The respective outputs of DE1 - DE12 are used to control the respective sampling operations of switches S5 - S16 in cycles K+13 through K+15.

In the next cycle of the RF input signal, namely cycle K+16, the SPS pulse will be back in proper position relative to the RF input signal for controlling switch S1, S5, S9 or S13 to sample at 0°. This is because, in this example, after 16 cycles (K through K+15) of the RF input signal, the SPS pulse now "lags" the RF input signal by 16 x 1/16 = 1 cycle, and is thus back in its "original" phase (i.e., its cycle K phase) relative to the RF signal. Accordingly, after cycle K+15, the operations in FIGURE 6 can, for example, return to cycle K and repeat (in which case the SPS pulse would control switch S1 again).

The router 17 can be readily implemented, for example, utilizing a passive pass gate design including a matrix of CMOS pass gates controlled by bits in a plurality of n-bit registers. In the example of FIGURE 6, a total of four n-bit registers can be used, each register corresponding to a respective one of the four routing schemes shown in

FIGURE 6. The registers can be sequentially enabled (one every 4th RF cycle) in the cyclic pattern illustrated in FIGURE 6.

FIGURE 7 illustrates exemplary operations which can be performed by the embodiments illustrated in FIGURES 1 - 6. At 71, the local oscillator frequency $F_{LO}$ is set to be less than the frequency $F_{RF}$ of the RF input signal, and a sample switch index i is set to 1. At 72, the sampling pulse signal SPS is produced from the local oscillator. At 73, the jth SPS pulse is selected as the current sample pulse, and is applied to switch Si at 74. For example, the jth SPS pulse can be applied to switch S1 in order to sample at 0°. Thereafter, if it is determined at 75 that switch Sn has not yet been operated, then the next switch is selected at 70 by incrementing the switch index i. Thereafter at 76, a new sample pulse is produced in response to the current sample pulse, for example by producing a delayed version of the SPS pulse that was selected at 73. At 77, the new sample pulse is selected as the current sample pulse, and the current sample pulse is applied to switch Si at 74. The above-described operations at 70 and 74 - 77 are repeated until it is determined at 75 that all n switches have been operated.

When it is determined at 75 that all n switches have been operated, at 79 the sampling switch index i is again set equal to 1, and the SPS pulse index j is incremented. It is thereafter determined at 78 whether the jth SPS pulse is in phase for the assigned

sampling operation of switch Si. If not, then the operations described above and illustrated at 76, 77 and 74 are sequentially executed in that order. Thereafter, the sampling switch index i is incremented at 80, after which it is determined at 78 whether the jth SPS pulse is in the appropriate phase for controlling the assigned sampling operation of switch Si. If not, then the aforementioned sequence of operations 76, 77, 74, 80 and 78 are repeated. However, if the jth SPS pulse is determined at 78 to be in the appropriate phase for controlling the assigned sampling operation of switch Si, then the jth SPS pulse is at 73 selected to be the current sample pulse. Thereafter, operations beginning at 74 are repeated again as described above.

FIGURE 8 illustrates exemplary operations which can be performed by the embodiments of FIGURES 1-6. After generation of an SPS pulse at 81, that pulse and delayed versions thereof are used at 82 to sample desired phases in adjacent cycles of the RF signal. The sampled phases are recombined at 83 to produce the desired downconverted signal.

As will be evident to workers in the art, the embodiments of FIGURES 1 - 8 can be used to realize a zero-IF or near-zero-IF receiver architecture wherein the frequency of the local oscillator is advantageously shifted away from the frequency of the RF input signal by a factor such as n/(n+1). For example, in the case of a Bluetooth receiver with

n=16, the oscillator frequency is 2.25 GHz for an RF input frequency of 2.4 GHz, and the oscillator frequency is 2.34 GHz for an RF input frequency of 2.5 GHz. Thus, the frequency of the local oscillator lies outside of the Bluetooth frequency band, which insures that any leakage from the local oscillator is suppressed by the Bluetooth antenna filter, and also insures that no other channel is folded into the downconverted signal. The local oscillator can therefore be advantageously integrated without the leakage problem of conventional arrangements. Also, the delay elements can be realized, for example, by a suitable inverter chain, which advantageously requires a much smaller silicon area than conventional polyphase networks. Furthermore, because all desired phases of each cycle of the RF input signal are sampled and recombined in the IF amplifier, there is no signal loss as compared to a conventional sub-sampling scheme. This is illustrated by FIGURE 9, which shows the in-phase path.

In some embodiments, the router 17 can control the switches 19 to generate an SC (switched capacitor) filter function during the phase sampling operations. In this manner, undesired interferers can be advantageously attenuated during the sampled-phase recombination operations of the IF amplifiers. An example of this is illustrated by FIGURE 10, wherein the switch activation sequence is modified as shown (S5 and S7 are

reversed with respect to the sequence of FIGURE 9) to support a desired SC filter function.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.